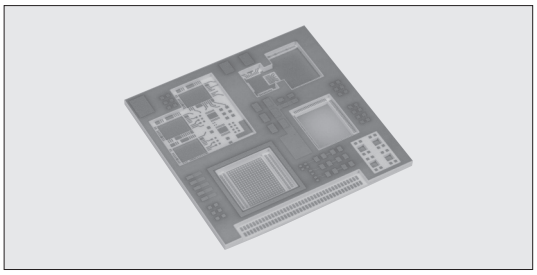
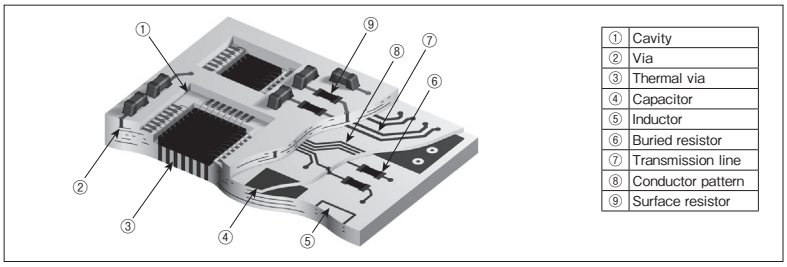
KLC LTCC Multilayer Substrates



■Construction



①	Cavity
②	Via
③	Thermal via
④	Capacitor
⑤	Inductor
⑥	Buried resistor
⑦	Transmission line
⑧	Conductor pattern
⑨	Surface resistor

■What is LTCC?

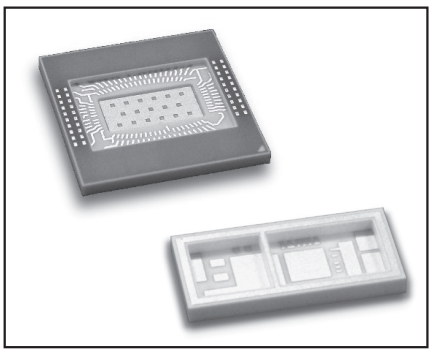
LTCC stands for Low Temperature Co-fired Ceramics.
KOA's LTCC are multilayer ceramic substrates. This technology permits to use low resistive material as conductor patterns due to the lower temperature needed during firing process compared to general ceramic firing process. This is achieved by adding glass to alumina.
KOA uses Silver based paste (Ag) to create the electrical structures in and on the ceramics layers. To be noted, that top and bottom layers patterns can be platted using various processes.
Thanks to these materials, low loss electrical performance can be achieved as well as high dimensional accuracy.
KOA's LTCC provides clear advantages for system downsizing by forming surface resistors, inner resistors, and transmission lines on/in the substrate. In addition, our thermal expansion coefficient is close to silicon's one, enhancing the reliability of mounted bare chip. Furthermore, cavity structures can be formed, making possible the creation of low profile packages.

■Features

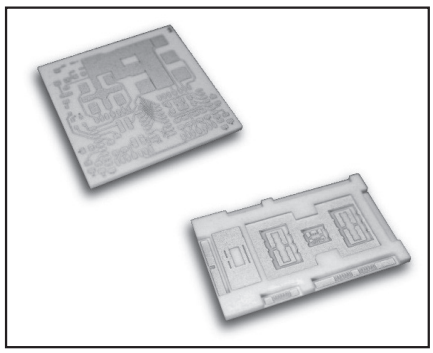
- KOA's substrates are suitable for bare chip mounting, as the thermal expansion cofficient is close to silicon's one and outstanding dimensional accuracy and flatness.
- Thanks to our low dielectric ceramics and low resistive conductors, the substrates excel in the high frequency characteristics.
- Minituarization and high integration are possible because of multiayer wiring, multi-cavity structure and the surface/buried printing resistors possibilities.
- Special shapes of substrate and cavity such as circle shape, polygonal shape and concave or convex shape are available.
- Thermal vias under bare chips can be implemented to improve the thermal conductivity of the substrate.
- The substrates are outstanding in heat resistance and humidity resistance. There will be no outgas occurrence from the ceramics.
- Products meet EU-RoHS requirements.

■Applications

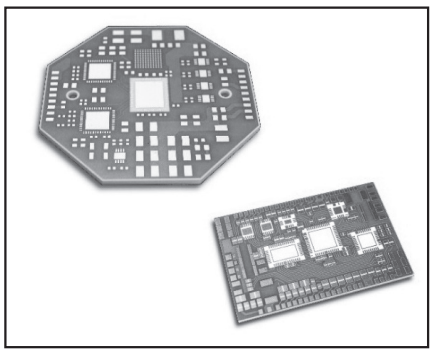
- Applications running at high frequencies like micro-waves, milli-waves, etc.
- Applications used in harsh environment, especially in high temperatures, high humidity, etc.
- Various sensor packages.
- Multi chip modules for bare chips.
- MEMS packages.
- Interposer substrates.



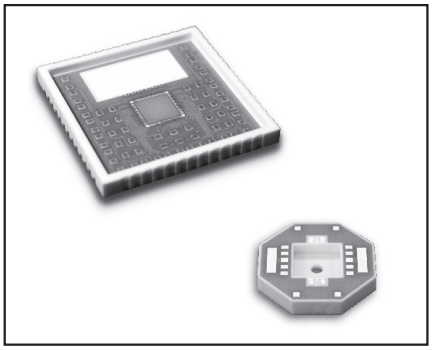
Sensor Module



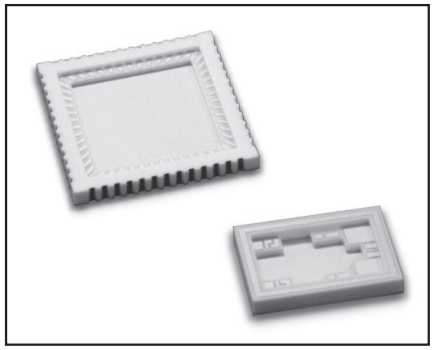
RF Module



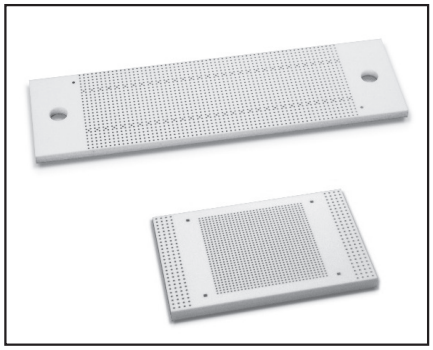
Multi Chip Module



MEMS Sensor Package



Various Device Package



Interposer Substrate

■Type Designation

Example

KLC	AB1
Product Code	KOA Ref. No.

Contact us when you have control request for environmental hazardous material other than the substance specified by EU-RoHS.

■Characteristics of Substrate Material

Parameter	Characteristics
Bending strength(MPa)	250
Thermal expansion coefficient($\times 10^{-6}$/K)	5.5
Thermal conductivity(W/m・K)	3
Insulation resistance(Ω・cm)	$>10^{13}$
Dielectric constant at 1GHz	6.6
Dielectric loss at 1GHz	0.004
Density(g/cm^3)	2.8
Surface roughness Ra(μm)	<0.4
Withstanding voltage(kV/mm)	>15
Substrate thickness(mm)	0.4~2.0 STD.
Layer thickness(μm/Layer)	80、100、125 STD.

■Conductor

Parameter	Characteristics
Material of conductor	Ag
Resistivity of conductor(μΩ・cm)	2.5
Surface plating	Ni-Au、Ni-Pd-Au

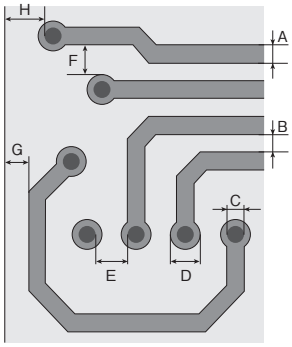
■Surface・Buried printed resistor

Parameter	Surface resistor	Buried resistor
Resistance Range (Ω)	10~100k	10~200k
Resistance tolerance (%)	±5	±20~50

■Design rule

Symbol	Parameter	Design value
A	Line width	0.06mm Min.
B	Line to line spacing	0.06mm Min.
C	Via diameter	0.1mm, 0.15mm, 0.2mm
D	Via pad diameter	Via diameter+0.05mm Min.
E	Via to via spacing	0.2mm Min.
F	Via pad to line spacing	0.125mm Min.
G	Part edge to conductor spacing	0.2mm Min.
H	Part edge to via spacing	0.3mm Min.
J1, J2	Cavity width	0.6mm Min.
K1, K2	Cavity depth	0.1mm Min.
L	Wall width of cavity	0.5mm Min.
M	Shelf width in the cavity	0.5mm Min.

Surface layer・Inner layer



Cavity